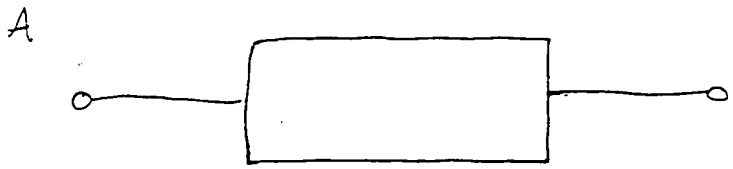


FIG 1.

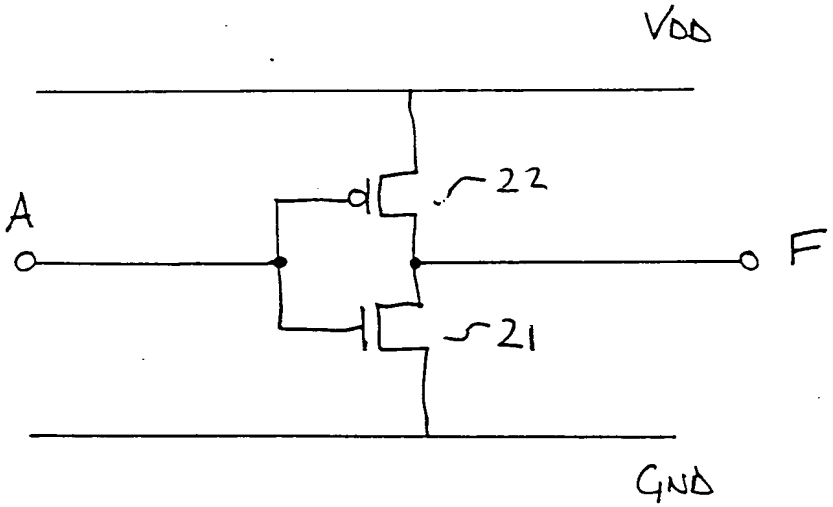


FIG 2.

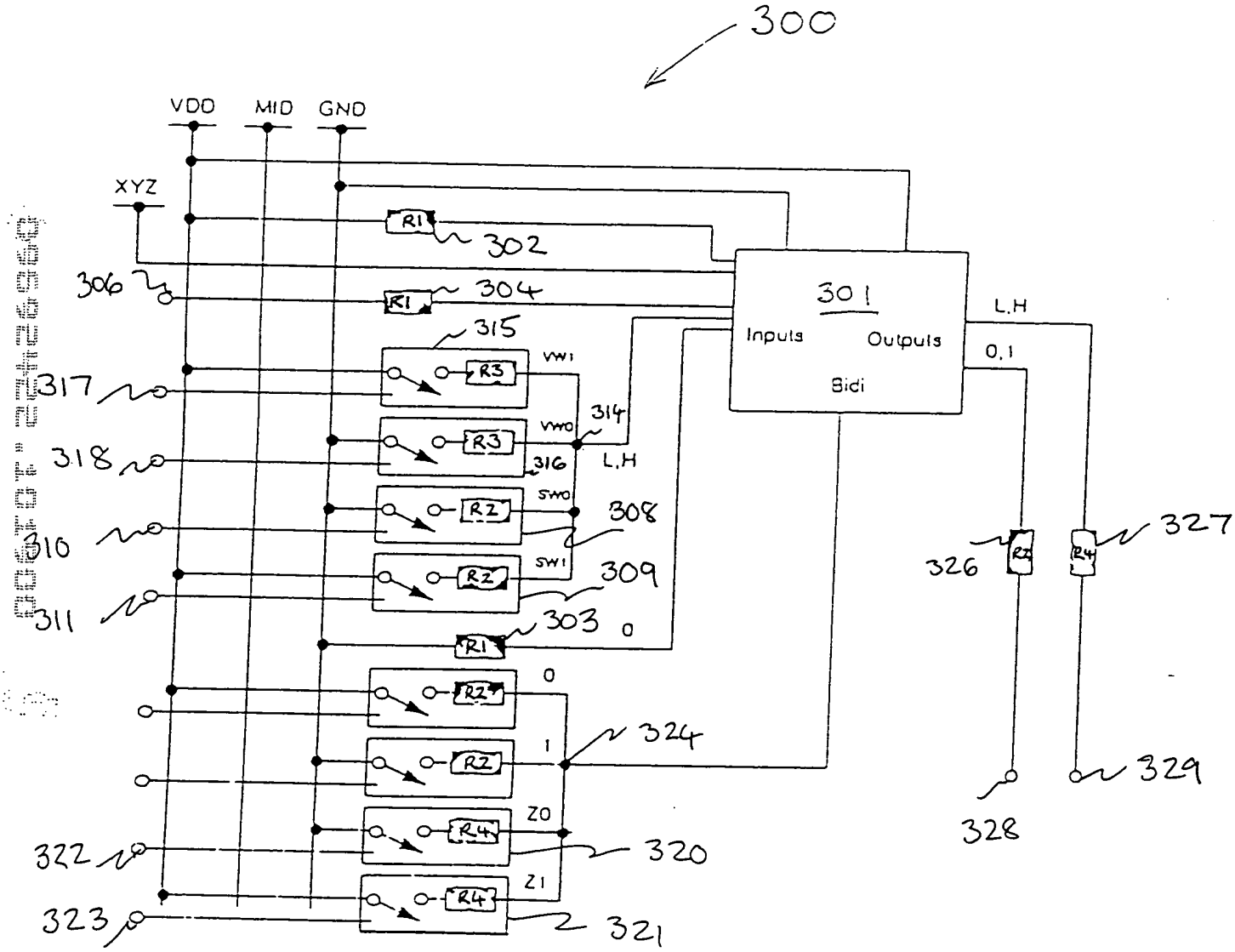

300
VDD
MID
GND
XYZ
R1
302
306
R1
304
301
Inputs
Outputs
Bidi
L,H
0,1
315
R3
VW1
317
R3
VW0
314
318
316
L,H
R2
SW0
308
310
R2
SW1
309
311
R1
303
0
R2
0
R2
1
324
R4
Z0
322
320
R4
Z1
323
321
326
R2
R4
327
328
329

FIG 3.

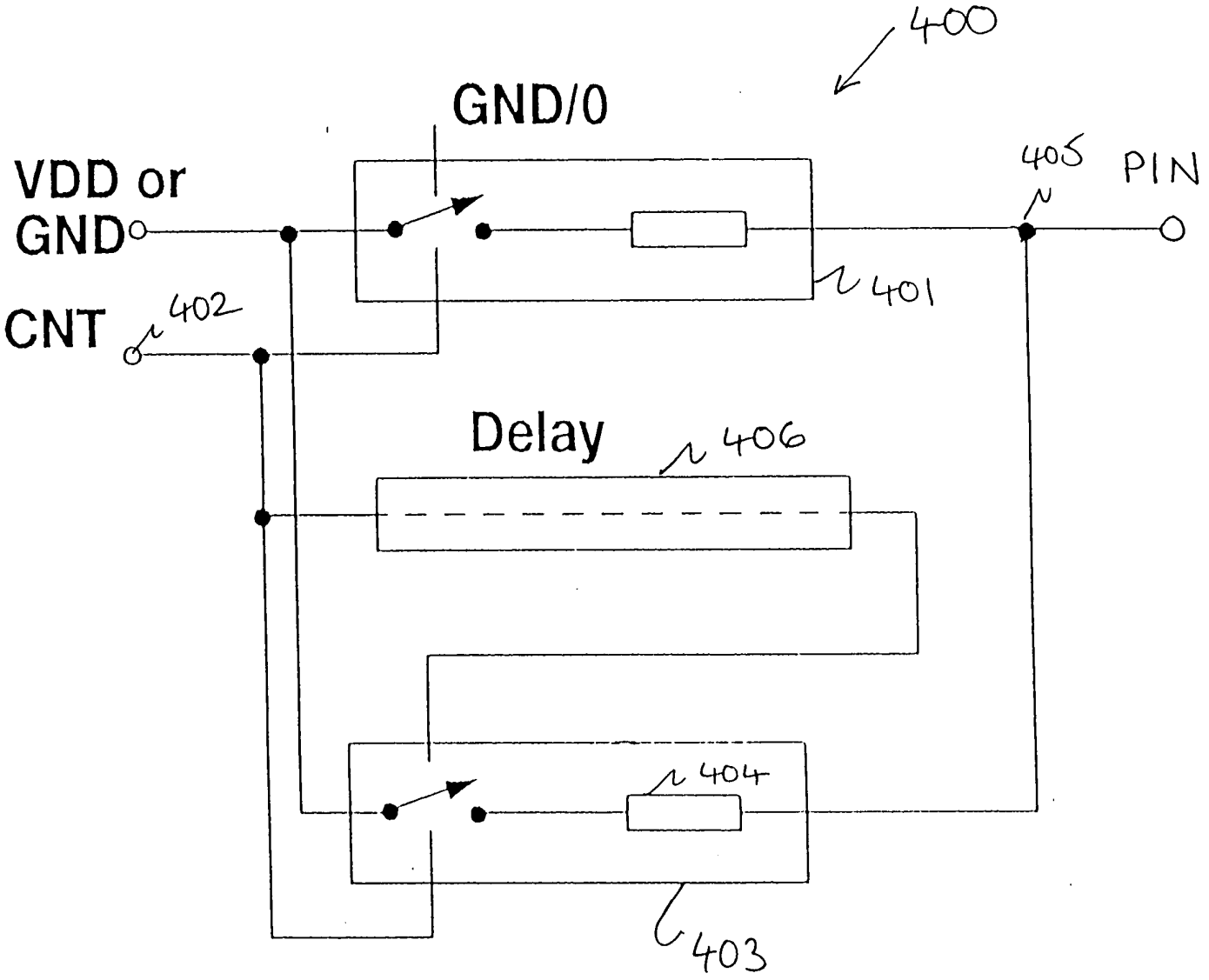
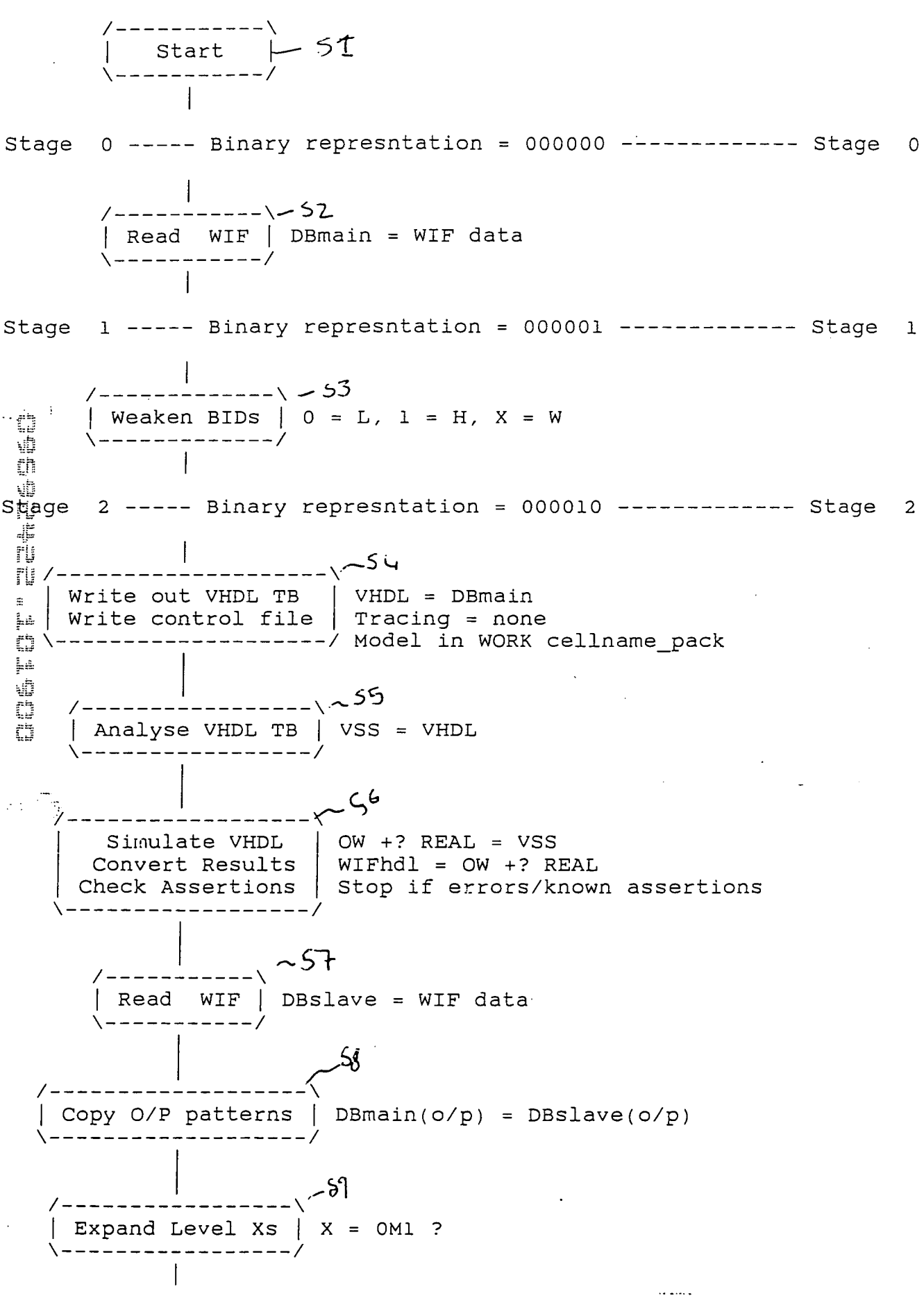


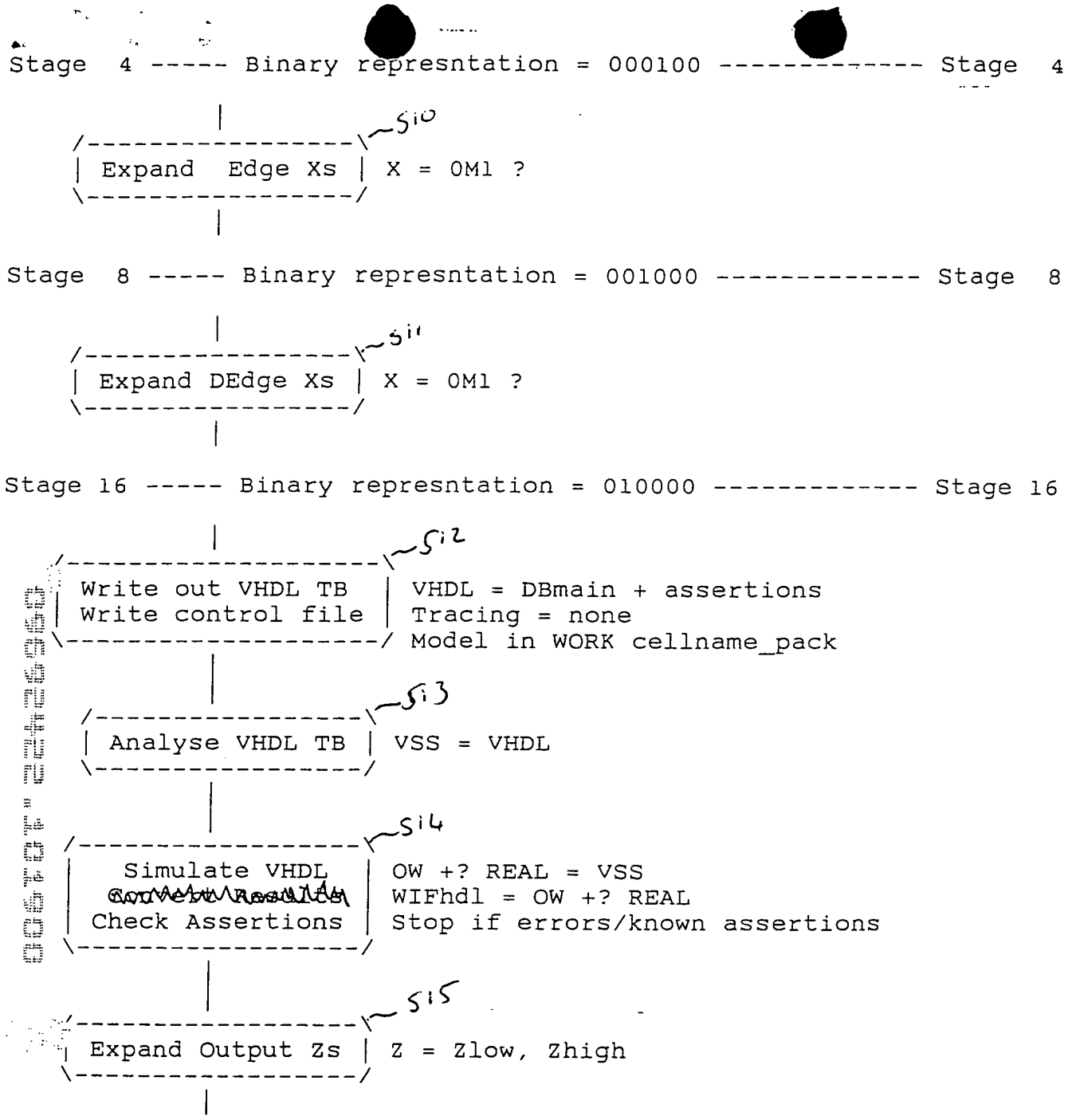
FIG 4.

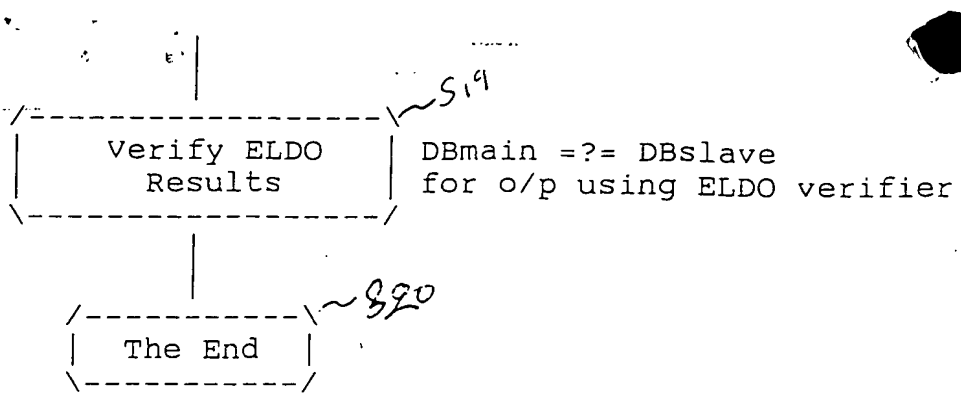
FIG 5.

FIGURE 6

WIF2TB Flow Diagram
==========




Stage 4 ----- Binary represntation = 000100 ---------- Stage 4
S10
Expand Edge Xs
X = 0M1 ?
Stage 8 ----- Binary represntation = 001000 ---------- Stage 8
S11
Expand DEdge Xs
X = 0M1 ?
Stage 16 ----- Binary represntation = 010000 ---------- Stage 16
S12
Write out VHDL TB
Write control file
VHDL = DBmain + assertions
Tracing = none
Model in WORK cellname_pack
S13
Analyse VHDL TB
VSS = VHDL
S14
Simulate VHDL
Convert Results
Check Assertions
OW +? REAL = VSS
WIFhdl = OW +? REAL
Stop if errors/known assertions
S15
Expand Output Zs
Z = Zlow, Zhigh
Stage 32 ----- Binary represntation = 100000 ---------- Stage 32
S16
Write out ELDO file
S17
Simulate ELDO
Convert Results
CHI = ELDO
WIFeldo = CHI
S18
Read WIF
DBslave = WIF data


Verify ELDO Results
DBmain =?= DBslave for o/p using ELDO verifier
The End